PRODUCTS AND LICENSING

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Revision History

Rev	Date	Comments
1.0	18.09.2014	First version

1 About This Document

This document gives an overview of the products that Flexibilis provides around the Flexibilis Redundant Switch (FRS) IP [1]. Based on this document, the FRS IP user should be able to notice other products that would add value on their end-product but also understand which products may be needed to generate designs.

Chapter 2 introduces the main FPGA IP Cores and Chapter 3 Protocol Stacks. Chapters 4 and 5 list additional SW and FPGA IP blocks that are available and Chapter 6 defines the available Reference Designs. Chapter 7 shows a product matrix for a couple of use cases and Chapters 8 and 9 define Abbreviations and References.

2 FPGA IP Cores

This chapter discusses Flexibilis IP blocks for FPGA designs and their licensing methods.

2.1 FRS IP

FRS [1] is an Ethernet switch IP block designed to be used in programmable environments. FRS includes multiple Ethernet Media Access Controller (MAC) functional entities and provides MII/GMII interfaces for Ethernet PHY devices and optionally for a host system CPU. FRS standard features include:

- 10/100/1000 Mbit/s Full-Duplex Ethernet interfaces
- Compatible with IEEE standard 802.1D MAC Bridges
- Media Independent Interfaces (MII) and Gigabit Media Independent Interfaces (GMII) for attaching to external Physical Layer devices (PHY) and host system CPU(s)
- Avalon slave interface for register access
- Ethernet packet forwarding at wire-speed, non-blocking
- PTPv2 end-to-end one-step transparent clock processing at hardware
- PTPv2 peer-to-peer transparent clock support functions
- PTPv2 boundary and ordinary clock support functions
- Ethernet packet filter and prioritization on each of the ports
- Compatible with IEC 62439-3 ”High-availability Seamless Redundancy (HSR)”
- Compatible with IEC 62439-3 ”Parallel Redundancy Protocol (PRP)”

2.1.1 Licensing

FRS IP is provided with the following licensing methods:

- **Royalty based black-box** design supporting 3-8 interfaces (requires a use separate security CPLD chip)
    - Altera: Cyclone IV, Cyclone V and Cyclone V SoC
    - Other vendors: not provided
    - For price and licensing information contact the local Altera representative
    - Available from https://www.altera.com/third-party/flexibilis/license/
    - Note: If External security CPLD is not present, the design will operate as a time-limited design.
- **Paid-up license** for FRS supporting 3-8 ports
    - Altera: Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
    - Xilinx: Spartan 6, Artix-7, Kintex-7. For other device families contact Flexibilis for more information
    - Lattice: For all device families contact Flexibilis for more information
    - Microsemi: Igloo2 and SmartFusion2. For other device families contact Flexibilis for more information
    - For price, licensing and availability information contact Flexibilis
    - For other vendors or Port configurations contact Flexibilis for more information

2.2 FES IP

The Flexibilis Ethernet Switch (FES) provides the same feature set as FRS, excluding PRP and HSR support.

2.2.1 Licensing

FES IP is provided with the following licensing methods:

- **Open Core Plus black-box** design for evaluation
    - Altera: No device family dependencies

    - Request core for evaluation from Flexibilis
    - Note: FRS IP may also be used in FES mode
- **Paid-up black-box** design supporting 3-12 ports
    - Altera: Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
    - Xilinx: Spartan 6, Artix-7, Kintex-7. For other device families contact Flexibilis for more information
    - Lattice: For all device families contact Flexibilis for more information
    - Microsemi: Igloo2 and Smartfusion2. For other device families contact Flexibilis for more information
    - For price, licensing and availability information contact Flexibilis
    - For other vendors or Port configurations contact Flexibilis for more information

2.3 FRTC IP

The Flexibilis Real-Time Clock IP [2] provides a real-time clock, which supports clock adjustment and provides the clock information via registers and external interface. In Addition, the FRTC supports Pulse Per Second (PPS) output signal for external synchronization.

2.3.1 Licensing

FRTC IP is provided with the following licensing methods

- **Open Core Plus black-box** design for evaluation
    - Altera: No device family dependencies
    - Available from www.flexibilis.com/downloads
- **Paid-up license** for FRTC
    - FRTC black-box design is provided free of charge for those using FRS IP royalty-based licensing. To get the license key, contact Flexibilis
    - Altera: Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
    - Xilinx: Spartan 6, Artix-7, Kintex-7. For other device families contact Flexibilis for more information
    - Lattice: For all device families contact Flexibilis for more information
    - Microsemi: Igloo2 and SmartFusion2. For other device families contact Flexibilis for more information
    - For price, licensing and availability information contact Flexibilis
    - For other vendors, contact Flexibilis for more information

2.4 AFEC IP

The Advanced Flexibilis Ethernet Controller (AFEC) IP [3] provides Ethernet MAC functionalities.

2.4.1 Licensing

AFEC IP is provided with the following licensing methods:

- **Open Core Plus black-box** design for evaluation
    - Altera: No device family dependencies
    - Available from www.flexibilis.com/downloads
- **Paid-up license** for AFEC
    - AFEC black-box design is provided free of charge for those using FRS IP royalty-based licensing. To get the license key, contact Flexibilis
    - Altera: Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
    - Xilinx: Spartan 6, Artix-7, Kintex-7. For other device families contact Flexibilis for more information
    - Lattice: For all device families contact Flexibilis for more information

- Microsemi: Igloo2 and Smartfusion2. For other device families contact Flexibilis for more information
- For price, licensing and availability information contact Flexibilis
- For other vendors, contact Flexibilis for more information

3 Protocol Stacks

Flexibilis provides a set of Protocol stacks, which are mainly targeted to be used with FRS IP.

3.1 XR7 PTP

The XR7 PTP stack [4] implements IEEE1588-2008 Precision Time Protocol (PTP) [5]. The XR7 PTP stack supports the following features [1]:

- Ordinary clock (OC, master and slave)
- Boundary clock (BC)
- Peer-to-Peer (P2P) delay measurements
- BMC algorithm
- Asymmetry corrections
- Configurable message intervals
- Support for multiple domains
- Different timescales (PTP, TAI, UTC)
- Layer 3 UDP multicast
- Layer 2 Ethernet multicast
- PTP management protocol (partial, not all messages)

3.1.1 Licensing

XR7 PTP is provided with the following licensing methods:

- **Paid-up source** code design
    - Available for the following environments:
        - Linux (Debian)
        - NIOS II (no OS)
    - For price, licensing and availability or support for different OS, contact Flexibilis
    - Note: XR7 PTP is provided free of charge for usage with FRS IP royalty-based licensing

3.2 Flexibilis Redundancy Supervision

Flexibilis Redundancy Supervision protocol stack [6] implements HSR/PRP Supervision protocol as specified in IEC 62439-3:2011 [7].

3.2.1 Licensing

Flexibilis Redundancy Supervision is provided with the following licensing methods:

- **Paid-up source** code design
    - Available for following environments:
        - Linux (Debian)
        - NIOS II (no OS)
    - For price, licensing and availability or support for different OS, contact Flexibilis
    - Note: Flexibilis Redundancy Supervision is provided free of charge when used with FRS IP royalty-based licensing

3.3 FRS Management Protocol Stack

FRS management protocol [8] is used to control FRS reference design over Ethernet. It is also possible to implement for example SNMP or NetConf agents that use the information provided by the protocol.

3.3.1 Licensing

FRS Management Protocol Stack is provided with the following licensing methods:

- **Paid-up source** code design
    - Available for the following environments:
        - Linux (Debian)
        - NIOS II (no OS)
    - For price, licensing and availability or support for different OS, contact Flexibilis
    - Note: FRS Management Protocol Stack is provided free of charge when used with FRS IP royalty-based licensing

4 Additional SW components and Environment

For Linux OS Flexibilis provides additional SW functionalities. Figure 1 describes different components and the dependencies between them.

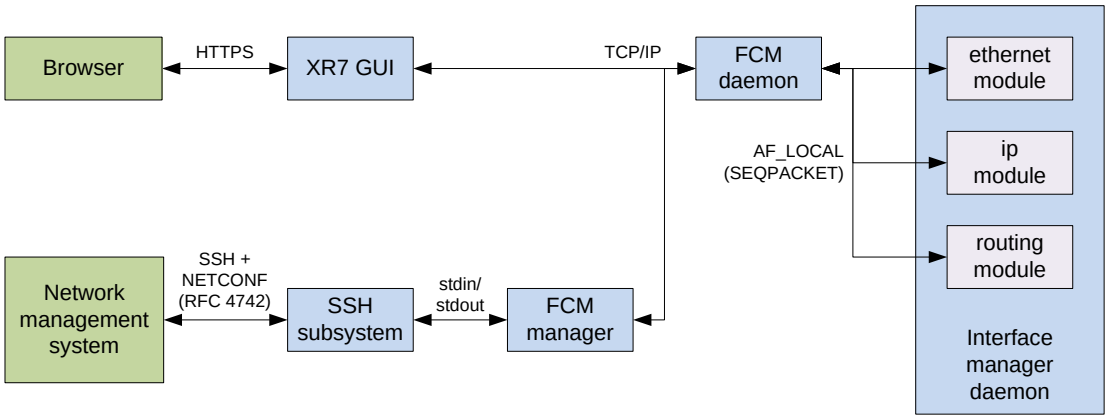

Figure 1. SW blocks

4.1 Flexibilis Configuration Manager Module and Daemon

Flexibilis Configuration Manager Daemon is an implementation of IETF NETCONF [9] network management protocol. FCMD design is modular. The daemon itself implements the protocol. The FCM modules, implemented as dynamically linked shared object libraries, provide NETCONF support for specific system components like PTP stack, Flexibilis Redundancy Supervision, network interfaces and so on.

4.1.1 Licensing

Flexibilis Configuration Manager Daemon and Module [10] is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for following environments:
    - Linux (Debian)
  - For price, licensing and availability or support for different OS, contact Flexibilis

4.2 Interface Manager

Interface Manager [11] is a daemon which provides NETCONF support for various network interfaces. Its design is modular – each module is implemented as a dynamically linked shared object library implementing FCM module interface.

4.2.1 Licensing

Interface Manager is provided with the following licensing methods:

- **Paid-up source** code design
  - Available for the following environments:
    - Linux (Debian)
  - For price, licensing and availability or support for different OS, contact Flexibilis

4.3 Graphical User Interface

XR7 GUI [12] provides web interface to the device for presenting status information and for configuring the system as desired by user. It is implemented as a Java servlet and it uses NETCONF to access the device resources.

4.3.1 Licensing

XR7 GUI is provided with the following licensing methods:

- **Paid-up source** code design
    - Available for the following environments:
        - Linux (Debian)
    - For price, licensing and availability or support for different OS, contact Flexibilis

4.4 XR7 Software Platform

Flexibilis XR7 software platform [13] is a complete system for building and managing GNU/Linux based firmware for devices. Devices can vary from more or less standard server PCs, embedded systems with a SoC to virtual machines. The platform is based on Debian and uses various Debian utilities and conventions. However, it uses them in a more specific way and presents an easy to use interface to them without sacrificing flexibility.

The Platform is available as a disk image, which can be used to setup multiple networked machines as needed. Machines can have a different firmware management related roles or overlapping roles but one machine acts as a software package repository server.

XR7 software platform provides the following features and services:

- Building software packages
    - Building software package means taking source code and compiling and linking it to binaries that can be used on target device. Cross-compiling is used when needed. Also files that do not need compiling can be packaged. Platform offers simple way to build packages either for testing during development or to be included in the firmware. Packages are built in robust, reliable, and reproducible way.
- Building device firmware
    - Firmware contains all software needed in a target device, in some target device specific format. Examples are SD-card images, NAND flash filesystem images, and so on. Platform offers simple way to create releases and needed firmware files. Detailed contents of each release are available and also accessible via HTTP using simple URLs.
- Small firmware upgrade packs
    - In many cases it is not desirable to replace the whole firmware on SD-card or NAND flash memory when doing system upgrades. Platform offers simplified way to create small upgrade packs, which provide new or upgraded packages or remove unneeded software packages from the firmware. Full customization of upgrade installation process is possible.
- Updating firmware of test system
    - Typically there are some devices in a dedicated test system or in lab. Platform offers a simple way to keep devices up-to-date by downloading and installing needed software from package repository server.
- Local Debian package archive
    - Platform manages software as Debian packages (.deb files). The package repository server acts as a local Debian package archive for upstream (Debian and Flexibilis) software as well as project specific software. New and upgraded software is sent to the package archive via SSH, and packages are available from the repository via HTTP. Many debugging and diagnostics utilities from Debian are available for use in test system devices, without needing to be included in official firmware.

- HTTP server
    - Package archive functionality uses HTTP, so Apache HTTP server is included in the platform. In each machine the HTTP server can also be used to configure other firmware related custom tasks.
- Continuous Integration (CI) server
    - Platform contains Jenkins CI server that can be used as needed. Its use is not required. Also external CI servers can be used for various firmware management tasks.
- DNS server
    - Typically there already is a DNS server for the development network and often it's best to use it to give names for platform servers (the package archive server, HTTP server virtual hosts). In some cases it may not be possible or desirable, so BIND DNS server is included with the platform.
- Multiple developer support
    - Many developers can use a single platform machine, or each developer can use his own machine. Any combination is also possible.

4.4.1 Licensing

XR7 Platform is provided with the following licensing methods:

- **Paid-up source** code design
    - Available for the following environments:
        - Linux (Debian)
    - For price, licensing and availability or support for different OS, contact Flexibilis

5 Additional FPGA IP cores

In addition to the IP cores listed in Chapter 2, Flexibilis also provides a few smaller IP cores to be used with the main Flexibilis IP cores.

5.1 Interface Adapters

As FRS/FES IP interfaces are GMII there is a selection of additional interface adapters that convert GMII to some other interface type. The following Interface adapters are provided:

- MII/GMII to SGMII/1000BASE-X
  - This adapter uses Altera's Triple Speed Ethernet which is a licensable product from Altera
- GMII to 1000BASE-X
- MII to 100BASE-FX
- MII/GMII to RGMII
- GMII to GMII
  - MAC-PHY GMII, swaps the TX clock direction
- GMII to EMAC
  - SoC EMAC, used in SoC FPGA designs

5.1.1 Licensing

Interface Adapters are provided with the following licensing methods:

- **Paid-up license** for Adapters
  - Note: Interface Adapters as black-box Designs are provided free of charge for those using FRS IP royalty-based licensing. To get the license key, contact Flexibilis.
  - Altera: Cyclone IV, Cyclone V and Cyclone V SoC. For other device families contact Flexibilis for more information
  - Xilinx: For all device families contact Flexibilis for more information
  - Lattice: For all device families contact Flexibilis for more information
  - Microsemi: For all device families contact Flexibilis for more information
  - These blocks are included in the Reference Design package, downloadable from www.flexibilis.com/downloads

5.2 Common Avalon blocks

A group of common Avalon blocks are provided to assist in QSYS designing:

- Avalon Terminate
  - Terminates an Open Avalon Master interface
- Avalon Arbit
  - Combines two Avalon masters i.e. transfers accesses from two slave interfaces to one master interface
- Avalon Export
  - Exports an Avalon interface from a QSYS block
- Avalon Splitter
  - Splits the Avalon address space. Used when the design includes multiple FRS IP Cores

5.2.1 Licensing

Common Avalon blocks are provided with the following licensing methods:

- **Paid-up license** for Common Avalon blocks
  - Note: Common Avalon blocks as black-box designs are provided free of charge for those using FRS IP royalty-based licensing. To get the license key, contact Flexibilis

- Supports any design using an interface that meets Avalon specification
- These blocks are included in the Reference Design package, downloadable from www.flexibilis.com/downloads

5.3 Miscellaneous blocks

Flexibilis also provides a group of miscellaneous blocks as listed below:

- Default Clock
  - Can be used instead of FRTC in TC only applications
- GMII Interconnect
  - For QSYS internal connections
- Authentication IF multiplexer
  - For applications with multiple FRS cores using the same security CPLD
- Link Led Control
  - Link LED functionality

5.3.1 Licensing

Miscellaneous blocks are provided with the following licensing methods:

- **Paid-up license** for Miscellaneous blocks
  - Note: Miscellaneous blocks as black-box designs are provided free of charge for those using FRS IP royalty-based licensing. To get the license key, contact Flexibilis
  - Supports any design and vendor
  - These blocks are included in the Reference Design package, downloadable from www.flexibilis.com/downloads

6 FRS Reference Design

Flexibilis provides FRS reference designs for evaluating the FRS IP. Mainly the reference designs can be divided into two categories: Reference designs with NIOS and reference designs with SoC ARM.

6.1 FRS Reference Design with NIOS

Reference Design with NIOS is provided for the following evaluation boards:

- Cyclone IV GX, DK-DEV-4CGX150N [14]
- Cyclone V GX, DK-DEV-5CGXC7NES [15]
- Cyclone V GT, DK-DEV-5CGTD9N [16]

The Reference design includes:

- Reference design **image** (flash file) including
    - FRS IP, time limited operation
    - AFEC IP
    - FRTC IP
    - NIOS with
        - XR7 PTP
        - Flexibilis Redundancy Supervision
        - FRS Management Protocol
        - Design related control SW
    - FRS related FPGA blocks (Interface adapters, Avalon bus components etc.) For more information check the Reference design specification
- Design related control SW **source codes** (component “drivers”, initializations etc.)
- FRS related FPGA blocks as **black-box** (Interface adapters, Avalon bus components etc.)
- Quartus Project files

Note: The reference design package does not include FRS IP, AFEC IP, FRTC IP or SW protocol stacks. To be able to recompile the design, these items are needed. The Reference design flash file can be used to configure the FPGA on the evaluation board.

6.2 FRS Reference Design with SoC ARM

Reference design with ARM is provided for the following evaluation boards:

- Altera Cyclone V SoC Development kit, DK-DEV-5CSXC6N [17]
- Terasic Cyclone V SoC Development kit [18]

Reference design includes:

- Reference design **image** (SD card image) including
    - FRS IP, time limited operation
    - AFEC IP
    - FRTC IP
    - Linux with
        - XR7 PTP
        - Flexibilis Redundancy Supervision
        - FCMs
        - Interface Managers
        - XR7 GUI
        - Kernel drivers
    - FRS related FPGA blocks (Interface adapters, Avalon bus components etc.) For more check the Reference design specification
- Kernal drivers, **source codes**
- FRS related FPGA blocks, **source codes** (Interface adapters, Avalon bus components etc.)

- Quartus Project files
- Note: The reference design package does not include FRS IP, AFEC IP, FRTC IP, SW protocol stacks, FCM, Interface manager or XR7 GUI. To be able to recompile the design, these items are needed. The Reference Design SD card image can be used to boot Linux and configure the FPGA on the evaluation board.

7 Product Matrix

7.1 Based on Functionality

The Product and availability matrix based on provided functionality is presented in Table 1.

	Quick Evaluation		Limited Design Evalution and Development	Full Functionality		
FPGA IP Cores						
FRS IP (/FES IP)	A	B	C	E	F	G
FRTC IP	A	B	C	F	G	
AFEC IP	A	B	C	F	G	
Protocol Stacks						
XR7 PTP	A	B		G		
Supervision	A	B		G		
FRS Management	A			G		
Linux SW Components						
FCM	B			G		
Interface Managers	B			G		
GUI	B			G		
Platform	B			G		
Others FPGA Components	A	B		D		

A	Reference Design Flash file. Downloadable from www.flexibilis.com/downloads
B	Reference Design SD card image. Downloadable from www.flexibilis.com/downloads
C	Time-limited, free of charge Evaluation version available from www.flexibilis.com/downloads
D	Full functionality, part of the reference design packages. Downloadable from www.flexibilis.com/downloads
E	Royalty-based (with CPLD chip).Contact Altera representative.
F	Paid-up black-box. Contact Flexibilis.
G	Paid-up source code. Contact Flexibilis.

Table 1. Product Matrix based on provided functionality

8 Abbreviations

Term	Description
AFEC	Advanced Flexibilis Ethernet Controller
CPU	Central Processing Unit
FCM	Flexibilis Configuration Manager
FPGA	Field Programmable Gate Array
FRS	Flexibilis Redundant Switch
FRTC	Flexibilis Real Time Clock
GMII	Gigabit Media Independent Interface
HSR	High-availability Seamless Redundancy
MAC	Media Access Controller
MII	Media Independent Interface
PPS	Pulse Per Second
PTP	Precision Time Protocol
PRP	Parallel Redundancy Protocol
SD	Secure Digital

9 References

[1] Flexibilis Redundant Switch (FRS) Manual, FRS_Manual.pdf

[2] FRTC User Manual, FRTC_user_manual.pdf

[3] Advanced Flexibilis Ethernet Controller (AFEC) User Manual, AFEC_user_manual.pdf

[4] XR7 PTP design specification, xr5_ptp_design.pdf

[5] IEEE standard 1588-2008

[6] Flexibilis Redundancy Supervision design specification, flx_redundancy_supervision_design.pdf

[7] Standard IEC 62439-3:2011

[8] FRS Management Protocol, FRS_management_protocol.pdf

[9] NETCONF, RFC 4741, http://tools.ietf.org/html/rfc4741

[10] Flexibilis Configuration Manager Design Specification, version 1.0.

[11] Interface Manager Release Notes

[12] XR7 GUI Design Specification, version 1.0

[13] XR7 Software Platform, Features and Overview. XR7platform_overview.pdf

[14] Cyclone IV GX FPGA Development Kit from Altera (ordering code DK-DEV-4CGX150N): http://www.altera.com/products/devkits/altera/kit-cyclone-iv-gx.html

[15] Cyclone V GX FPGA Development Kit from Altera (ordering code DK-DEV-5CGXC7NES): http://www.altera.com/products/devkits/altera/kit-cyclone-v-gx.html

[16] Cyclone V GT FPGA Development Kit from Altera (ordering code DK-DEV-5CGTD9N): http://www.altera.com/products/devkits/altera/kit-cyclone-v-gt.html

[17] Altera Cyclone V SoC Development kit, http://www.altera.com/products/devkits/altera/kit-cyclone-v-soc.html

[18] Terasic Cyclone V SoC Development kit, http://www.terasic.com.tw/cgi-bin/page/archive.pl?CategoryNo=167&No=816